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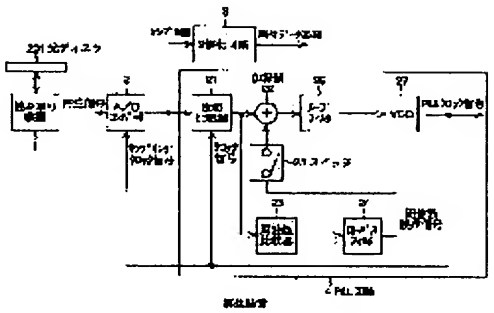
(54) CONVERTER AND METHOD, AND PLL ARITHMETIC UNIT AND METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To realize a digital PLL(phase-locked loop) circuit utilizing a frequency error.
SOLUTION: An A/D converter 2 samples a reproduction signal from a reader 1 synchronously with a clock signal from a PLL circuit 4 and the sampled value is outputted to a binarization circuit 3 and a phase comparator 21. The phase comparator 21 detects a change of the sampled value from a positive to a negative or vice versa (zero cross), and a phase error signal corresponding to the zero cross is outputted to a frequency comparator 23. The frequency comparator 23 provides an output of a frequency error detected by the change in the signal to a switch 25 via a low pass filter 24. The switch 25 provides an output of the frequency error to an adder 22 only when synchronization is locked. The adder 22 provides an output of a sum of the frequency error and the phase error to a VCO 27 via a loop filter 26. The VCO 27 oscillates a clock signal with a frequency corresponding to the value and gives it to the A/D converter 2 or the like.



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